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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,894	03/31/2004	Stephen H. Tang	INTEL-0056	4982

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EXAMINER	
PHAN, TRONG Q	

ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,894	TANG ET AL.	
	Examiner	Art Unit	
	TRONG PHAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-20 and 22-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-20 and 22-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's arguments in the Appeal Brief filed on 2/20/07 are persuasive in view of Oliver, 4,567,577, does not disclose the forward body bias.

However, in view of the newly discovered prior arts of De et al., 6,593,799, and Sano et al., 4,901,285, a new non-final office action has been set forth as follow:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-20 and 22-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura et al., 5,365,475, in view of Sano et al., 4,901,285 and De et al., 6,593,799.

Matsumura et al., 5,365,475, in Fig. 3 a static random access memory (SRAM) device (2) which can be usable as in SRAM mode/ACTIVE mode and as in ROM (two-phase ROM) storing any data (see lines 11-13, column 4) while read-only memory cell fixedly storing any data not being read (see lines 46-52, column 4) comprising:

Regarding claims 1 and 30:

a first transistor pair (transistors 21 and 23) coupled between a supply voltage line (27) and GROUND (28);

a second transistor pair (transistors 22 and 24) coupled between the supply voltage line (27/28) and GROUND (G1/G2), the supply voltage line to receive a first supply voltage

(V1) based on a first mode (SRAM mode/ACTIVE mode) of the memory device and to receive a second supply voltage (V2) based on a second mode (ROM mode storing any data) of the memory device, the second supply voltage (V2) being different than the first supply voltage (V1);

a first access transistor (transistor 25) coupled to a word line (WL), a first bit line (BL) and a common node (NA) of the second transistor pair (transistors 22 and 24);

a second access transistor (transistor 26) coupled to the word line (WL), a second bit line ($\overline{BL}$) and a common node (NB) of the first transistor pair (transistors 21 and 23);

Regarding claim 8:

the one transistor of the first transistor pair (transistors 21 and 23) comprises a PMOS transistor PMOS transistor 21) and the one transistor of the second transistor pair (transistors 22 and 24) comprises another PMOS transistor (PMOS transistor 22);

Regarding claim 9:

A static random access memory (SRAM) device (2) comprising:

a first SRAM memory cell having a cross-coupled inverter configuration,

the cross-coupled inverter configuration including at least four transistors (transistors 21, 23, 22 and 24);

a supply voltage line to provide a first supply voltage (V1) to two transistors (transistors 21 and 22) of the at least four transistors (transistors 21, 23, 22 and 24) of the first SRAM memory cell based on a first mode (SRAM mode/ACTIVE mode) of the first SRAM memory cell and to provide a second supply voltage (V2) to the two transistors (transistors 21 and 22) based on a second mode (ROM mode storing any data) of the

first SRAM memory cell, the second supply voltage (V2) being different than the first supply voltage (V1);

Regarding claim 10:

a power control unit (program unit 27) to change the supply voltage on the supply voltage line based on either the first mode or the second mode of the first SRAM memory cell;

Regarding claim 11:

the power control unit (program unit 27) further to control switching of the switching device based on either the first mode or the second mode of the first SRAM memory cell;

Regarding claim 16:

further comprising a second SRAM memory cell having a cross-coupled inverter configuration, the cross-coupled inverter configuration of the second SRAM memory cell including at least four transistors, the supply voltage line to provide a supply voltage to two transistors of the at least four transistors of the second SRAM memory cell based on a mode of the second SRAM memory cell (a plurality of SRAM cells 2 in Fig. 2A);

Regarding claim 18:

An electronic system comprising:

a processor device to process data (micro processor 104 in Fig. 15);

a static random access memory (SRAM) device (SRAM cell 2) to store the data;

and a power control unit (program unit 27) to control a supply voltage level (V1 and V2) applied to the SRAM device and to provide a signal indicative of

a mode of the SRAM device, the power control unit (program unit 27) to apply a first voltage level (V1) in a first mode (SRAM mode/ACTIVE mode) and to apply a second voltage level (V2) in a second mode (ROM mode storing any data), the SRAM device;

Regarding claim 35:

the first supply voltage V1) and the second supply voltage (V2) are applied to a source of the one transistor (transistor 21) of the first transistor pair (transistors 21 and 23) and to a source of the one transistor (transistor 22) of the second transistor pair (transistors 22 and 24);

Regarding claim 36:

the supply voltage line (27) to provide the first supply voltage (V1) and the second supply voltage (V2) to sources of the two transistors (transistors 21 and 22) of the at least four transistors (transistors 21, 23, 22 and 24) of the first SRAM memory cell 2);

Regarding claim 37:

the power control unit (program unit 27) to apply the first voltage level (V1) and the second voltage level (V2) to sources of transistors (transistors 21 and 22) within the SRAM device (2).

Matsumura et al., 5,365,475, discloses everything except the STANDBY mode (non-ACTIVE mode) recited in claims 1, 22-29 and 31-34.

Sano et al., 4,901,285, discloses in Figs. 1A, 1B the teaching that "during operation of ROM 10 while not being read (standby mode)" (see lines 36-37, column 4).

Therefore, in view of the above teaching of Sano et al., 4,901,285, the operation in which ROM (two-phase ROM) storing any data (see lines 11-13, column 4) while

read-only memory cell fixedly storing any data not being read (see lines 46-52, column 4) would have been obvious a STANDBY mode (non-ACTIVE mode) recited in claims 1, 22-29 and 31-34.

Matsumura et al., 5,365,475, which is modified by Sano et al., 4,901,285, disclose everything except the bias transistor comprising an NMOS coupled to a body of one of transistor of the first transistor pair and to a body of one of transistor of the second transistor pair, having a source coupled to GROUND to apply a forward body bias to the one of transistor of the first transistor pair and to the one of transistor of the second transistor pair based on a STANDY signal recited in respective claims 1-4, 6-20 and 22-37.

De et al., 6,593,799, discloses in Fig. 7 the teaching of using NMOS transistor 352 coupled between the bodies of PMOS transistors 340 and 342 and GROUND Vss to apply a forward body bias to each of PMOS transistors 340 and 342 in response to output of logic low voltage of control circuitry 516 in standby mode (see lines 2-6, column 2; lines 15-17 and 32-34, column 6) in a static memory SRAM device (see lines 29-30, column 1).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the NMOS transistor 352 in Fig. 7 of De et al., 6,593,799, for providing a forward body bias to each of PMOS transistors 21 and 22 in Fig. 3 of Matsumura et al., 5,365,475, which is modified by Sano et al., 4,901,285, for the purpose of obtaining high performance/high power or moderate performance/low power (see lines 55-58, column 10 of De et al., 6,593,799)

and increasing static noise margin (claim 20) (see lines 9-11, column 8 of De et al., 6,593,799).

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

phan 05/05/07

TRONG PHAN
PRIMARY EXAMINER